IN THE CLAIMS

At page 4 before the BRIEF DESCRIPTION OF THE DRAWINGS section, please insert the following:

BRIEF SUMMARY

A method and apparatus for efficient memory allocation and system management interrupt handling is herein described. In one embodiment, a single SMI is used to initialize each processor in a multi-processor environment. In addition, a location of a default SMI handler may be used as a wake-up vector to inactive processors to efficiently utilize memory. In another embodiment, unified handler code is executed on multiple processors to handle software generated SMIs.

At page 3, please make the following amendments to paragraph [0007]

[0007] However, these inefficient methods of initialization and handling are not limited to multiprocessor server systems, but exist in other systems, such as mobile multiprocessor systems. Hyper-Threading Technology (HT) is a technology from Intel.RTM. Corporation of Santa Clara, Calif. that enables execution of threads in parallel using a ~~signal~~ single physical processor. HT incorporates two logical processors on one physical processor (the same die). A logical processor is an independent processor visible to the operating system (OS), capable of executing code and maintaining a unique architectural state from other processor in a system. HT is achieved by having multiple architectural states that share one set of execution resources.

At page 7, please make the following amendments to paragraph [0023]

[0023] FIG. 1 illustrates a block diagram of a device 105 with multiple logical processors. A physical processor refers to a physical processor die or a single package. A logical processor is an

independent processor visible to the operating system (OS), capable of executing code and maintaining a unique architectural state from other processor in a system. Hyper-Threading Technology (HT) is a technology from Intel.RTM. Corporation of Santa Clara, Calif. that enables execution of threads in parallel using a ~~signal~~ single physical processor. HT includes two logical processors on one physical processor and is achieved by duplicating the architectural state, with each architecture state sharing one set of processor execution resources.